IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 5 with the following new paragraph:

The present invention relates to the field of programmable single-chip systems [on a chip (PSoCs)]. Specifically, the present invention relates to a software program which allows a circuit designer to configure a circuit and then automatically generate a series of items to facilitate programming a microcontroller.

Please replace the paragraph beginning at page 6, line 9 with the following new paragraph:

Figure 6A, Figure 6B, Figure 6C, and Figure 6D are illustrations of graphical user interfaces for configuring interconnections between [PSoC] programmable system blocks, according to an embodiment of the present invention.

Please replace the paragraph beginning at page 10, line 5 with the following new paragraph:

Referring now to Figure 1B, a user module placement work-space includes a resource graphic window 360 illustrating the placement of user modules 304 with respect to the available resources (e.g., available [PSoC] programmable system blocks 410 of a microcontroller) in a hardware layout graphical display. Throughout this application the term resource image may denote the blocks 410 upon which user modules 304 are placed in window 360. As the resource images may represent [PSoC] programmable system blocks in one embodiment, the resource images may be referred to as [PSoC] programmable system blocks for convenience. It will be understood that the resource images may represent other resources however, as the present invention is not limited to implementing the user modules 304 in [PSoC] programmable system blocks. Figure 1B shows a number of digital [PSoC] programmable system blocks 410a along the top row (e.g., the blocks labeled DBA00, DBA01, etc.), as well as four columns of analog [PSoC] programmable system blocks 41 0b (e.g., the blocks labeled ACA00, ACA01, etc.). The present invention is well suited

to using any number of analog and digital [PSoC] programmable system blocks 410. Furthermore, the blocks in graphic window 360 are not limited to representing [PSoC] programmable system blocks.

Please replace the paragraph beginning at page 10, line 22 with the following new paragraph:

A single user module 304 may map to one or more [PSoC] programmable system blocks 410. Color coding (not shown) may be used to relate the user modules 304 of selected modules window 306 with their schematic placement in resource graphic window 360. The analog 410b and digital 410a [PSoC] programmable system blocks may be more generally defined as two different classes to which a user module 304 maps. The present invention is well-suited to having many different classes.

Please replace the paragraph beginning at page 11, line 4 with the following new paragraph:

Referring now to Figure 1C, a pin-out configuration work-space is shown. The pin-out configuration work-space allows the user to connect [PSoC] programmable system blocks 410 to input/output (I/O) pins, as well as configure the I/O pins' drive characteristics. In one embodiment, a pin configuration window 380 may be used to configure pins. Pin configuration window 380 has a port column 381, a select column 382, and a drive column 383. In another embodiment, a user may [to] set pin configurations by clicking on the GUI of the chip 610. The operation of these features will be discussed more fully herein.

Please replace the paragraph beginning at page 12, line 17 with the following new paragraph:

Referring now to step 230 of Figure 2, in response to a request from a user for a potential (e.g., valid) position for a selected user module 304, a position is computed. The computer automatically determines the possible placements based on the available resources and the number

of [PSoC] programmable system blocks 410 and the types of [PSoC] programmable system blocks 410 that are required for the unplaced user module 304. Because the user does not need to determine the potential placements, designing the circuit is faster and less error prone than conventional methods which do not provide such guidance.

Please replace the paragraph beginning at page 13, line 2 with the following new paragraph:

User modules 304 may require multiple [PSoC] programmable system blocks 410 to be implemented. In some cases, user modules 304 may require special ports or hardware which may limit which [PSoC] programmable system blocks 410 can be used for their implementation. The process of mapping a user module 304 to [PSoC] programmable system blocks 410, such that the user module 304 is realized within the microcontroller, may be referred to as "user module placement." An embodiment automatically determines the possible placements of a user module 304 based on an Extensible Markup Language (XML) user module description and the hardware description of the underlying chip. However, the present invention is not limited to using XML descriptions. The potential placement positions may be automatically inferred based on the XML input data. Therefore, the placement process of embodiments of the present invention is data driven.

Please replace the paragraph beginning at page 13, line 15 with the following new paragraph:

In step 240, one or more [PSoC] programmable system blocks 410 are highlighted to indicate a possible position for the user module 304 based on, for example, XML input data. The placement is shown in a graphical hardware layout diagram 360 by highlighting the [PSoC] programmable system blocks 410 involved. For example, referring to Figure 1B, the ADCINC12_1 user module 304 has been selected for placement in the window 360. This user module 304 requires two digital blocks 410a and one analog block 410b. The digital [PSoC] programmable system blocks 410a labeled DBA00 and DBA01 are highlighted to indicate a possible position for the ADCINC12_1

user module 304. Referring now to Figure 3A, the analog [PSoC] programmable system block [410a] 410b labeled ASB20 is highlighted to indicate that it is a possible position for the analog portion of the ADCINC12_1 user module 304. Embodiments may use color coding to associate the highlighting color with a unique color assigned to that user module 304.

Please replace the paragraph beginning at page 14, line 4 with the following new paragraph:

User module placement is described in co-pending US patent application serial number [_____] 09/989,762, filed concurrently herewith, entitled "A SYSTEM AND METHOD FOR PERFORMING NEXT PLACEMENTS AND PRUNING OF DISALLOWED PLACEMENTS FOR PROGRAMMING AN INTEGRATED CIRCUIT," by Ogami et al., attorney docket number CYPR-CD01175M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 14, line 11 with the following new paragraph:

Referring now to Figures 3A-3C and to step 250 of Figure 2, after placing a user module 304, a user may desire to move it to another [PSoC] programmable system block 410 (or blocks). In step 250, a new possible position for a user module 304 is computed, in response to a user request for a new position for the user module 304. The user may select a next position button 371 to cause this to occur. Figures 3A-3C illustrate three possible positions for the analog portion of the ADCINC12_1 user module 304. The user may then click on a place module button 372 to place the module 304. Placements that are incompatible with the user module requirements (e.g., characteristics) are automatically pruned out by the software and therefore are not displayed as valid placements. In one embodiment, all positions are shown to the user, sequentially, each time the next placement icon 371 is selected. However, if a potential placement involves a [PSoC] programmable system block 410 that has already been used (e.g., by another placed user module 304), then in these

cases the place user module [372] icon 372 is grayed out indicating that this placement is only valid if the resources were vacant. This allows the user to see all possible placements.

Please replace the paragraph beginning at page 15, line 24 with the following new paragraph:

User module next placement is described in co-pending US patent application serial number [_____] 09/989,781, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR DECOUPLING AND ITERATING RESOURCES ASSOCIATED WITH A MODULE," by Ogami et al., attorney docket number CYPR-CD01180M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 16, line 6 with the following new paragraph:

Steps 210 through 250 may be repeated to allow the user to add more user modules 304. Each time a new user module is selected, a system resource window may be updated. Referring again to Figure 1A, for each user module 304 selected, the system updates the data in the Resource Manager window 350 with the number of occupied [PSoC] programmable system blocks 410, along with RAM and ROM usage used by the current set of "selected" user modules 304. The system may also prevent a user from selecting a user module 304 if it requires more resources than are currently available. Tracking the available space and memory of configurations for the design may be performed intermittently during the whole process of configuring the microcontroller. Embodiments provide a live graph tracking the [PSoC] programmable system blocks 410 used by percentage. The RAM and ROM monitors may track the amount of RAM and ROM required to employ each selected user module 304.

Please replace the paragraph beginning at page 16, line 19 with the following new paragraph:

After the user has selected one or more user modules 304, the user may select global parameters and user module parameters such as, for example, the gain of an amplifier, a clock speed, etc. Referring now to Figure 4 and to step 260 of Figure 2, in response to a user clicking on a region on a [PSoC] programmable system block 410 an interface 510 is displayed which allows the setting of user module parameters. For example, the user may place "the cursor" over the lower-left corner of a [PSoC] programmable system block 410 to set input parameters. The system may display a superficial chip or a changed cursor in response to this. The user may then left-click a mouse, for example, to bring up a user [moldule] module parameter window 510 to configure the user module input parameters. The process may be repeated in the lower-right corner of the [PSoC] programmable system block 410 for output parameters and on the upper-left corner for clock parameters. The present invention is not limited to these steps for bringing up a user module pop-up window 510, however. The system may then display the selected parameters in a user module parameter window 520. Various pop-up windows may be data driven in that the contents of the pop-up window may depend on, for example, the user module 304 selected. Alternatively, user parameters may be set in the user module parameter window 520.

Please replace the paragraph beginning at page 17, line 12 with the following new paragraph:

When the user module 304 is placed (e.g., instantiated) on a particular [PSoC] programmable system block 410 the register settings and parameter settings may be mapped to a physical register address on the chip. This may also associate interrupt vectors that the user module 304 uses based on the [PSoC] programmable system block 410. Each of the digital blocks 410a maps to one vector and each column of analog blocks 410b maps to one vector. Once the user modules 304 are placed and the parameters are set, all the physical address registers that are associated with that user module 304 are fixed and the register values are determined.

Please replace the paragraph beginning at page 19, line 7 with the following new paragraph:

Pin configuration is described in co-pending U.S. patent application serial number [_____] 10/032,986, filed October 29, 2001, entitled "PIN-OUT CONNECTIONS/DRIVE LEVELS DIRECT-SET BY DROP DOWN LIST," by Ogami et al., attorney docket number CYPR-CD01173M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 19, line 13 with the following new paragraph:

Referring now to Figure 6A-6D and to step 280 of Figure 2, embodiments provide many different windows to assist the user in setting various parameters to 1 specify interconnectivity of [PSoC] programmable system blocks 410. Referring to Figure 6A, the user may cause window 605 to appear to configure the analog output buffer. Referring to Figure 6B, the user may cause a clock window 606 to appear by clicking on a clock MUX 616 to configure which clock will be the input to a column of analog [PSoC] programmable system blocks 410b. Referring to Figure 6C a port selection window 607 is shown. The port selection window 607 may be made to appear by clicking on or near the pin input MUX 608. The user may then select the input port. Referring now to Figure 6D, the user may click on or near the analog clocking MUX 614 to cause a window 613 to appear to select which digital [PSoC] programmable system block 410a should be selected by the clock MUX (616 of Figure 6B).

Please replace the paragraph beginning at page 20, line 16 with the following new paragraph:

Embodiments automatically generate source code files for realizing the user modules within the [PSoC] programmable system blocks 410 in the chip. Throughout this application the term source code may be defined as the code that is used to program registers on the chip to implement the selected user modules 304 as they have been placed by the user and to configure the [PSoC]

programmable system blocks to operate with the user selected parameters, interconnections, and pin-outs. Thus, automatically generated source code programs may realize the user modules 304 within the [PSoC] programmable system blocks 410.

Please replace the paragraph beginning at page 21, line 1 with the following new paragraph:

The automatically generated files may be programmed into flash memory of a target device (e.g., a microcontroller). The flash memory may then be used to program registers on the target device in order to implement a particular user module 304 in hardware (e.g., actual [PSoC] programmable system blocks 410). Therefore, the source code may be generated based on the selection, placement, and configuration of the user modules 304. For example, the automatic code generation processes take into account the parameterization of the user modules 304 and the placement of the user modules 304, which the user may perform via a GUI of embodiments of the present invention.

Please replace the paragraph beginning at page 21, line 23 with the following new paragraph:

Automatic generation of source code files is described in co-pending US patent application serial number [_____] 09/998,848, filed November 15, 2001, entitled "DESIGN SYSTEM PROVIDING AUTOMATIC SOURCE CODE GENERATION FOR PERSONALIZATION AND PARAMETERIZATION OF USER MODULES," by Ogami, attorney docket number CYPR-CD01177M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 22, line 7 with the following new paragraph:

After the microcontroller has been configured to implement the selected user modules 304, the user may wish to program desired functionality into the microcontroller. For example, a user

may wish the user modules 304, now implemented in [PSoC] programmable system blocks in hardware, to function in a certain fashion when the microcontroller is being used. Embodiments automatically generate APIs, which can be used to perform common functions that are required to interact with the user module (e.g., how to start the timer, how to stop the timer, how to talk to the timer, etc.) from an application program level. For example, a user may insert an API into a software program which he writes. Thus, one type of API may be described as a function call; however, APIs are not limited to function calls.

Please replace the paragraph beginning at page 23, line 6 with the following new paragraph:

Automatic generation of API files may take into consideration the configuration the user made. For example, the values to which certain registers are set may depend on which block 410 the user module 304 is placed in. Figure 9A and Figure 9B illustrate an exemplary API file that is automatically generated for a user module ADCINC12_1. This file contains the actual code for the API. Figure 10 and Figure 11 illustrate two more exemplary API files that may be generated for a user module named ADCINC12_1. Each instantiation of each user module 304 may have such files automatically generated for it. The file in Figure 10 may be used to allow programs written in the C programming language to access the user module APIs. The file of Figure 11 contains equates that are used by the APIs. The APIs simplify the designer's task by declaring values for various registers based on the [PSoC] programmable system blocks 410 the user module 304 occupies.

Please replace the paragraph beginning at page 24, line 4 with the following new paragraph:

Automatic generation of APIs is described in co-pending US patent application serial number [_____] 09/994,599, filed concurrently herewith, entitled "AUTOMATIC API GENERATION TO FUNCTIONAL [PSOC] PROGRAMMABLE SYSTEM BLOCKS," by Ogami et al., attorney

docket number CYPR-CD01198M and assigned to the assignee of the present invention and incorporated herein by reference.

Please replace the paragraph beginning at page 27, line 9 with the following new paragraph:

Automatic generation of datasheets is described in co-pending US patent application serial number [_____] 09/994,600, filed concurrently herewith, entitled "SYSTEM AND METHOD FOR DYNAMICALLY GENERATING A CONFIGURATION DATASHEET," by Ogami et al., attorney docket number CYPR-CD01174M and assigned to the assignee of the present invention and incorporated herein by reference.

IN THE DRAWINGS

Applicant respectfully requests approval of the drawing changes proposed in the enclosed Request for Approval of Drawing Changes.

SUPPORT FOR AMENDMENTS

Support for the amendments herein can be found throughout the specification (e.g., page 1, lines 5-8), Title and Abstract as originally filed, and in the copending applications cited in the specification. The present amendment intends to remove references to the trademarks of Cypress MicroSystems, Inc. (see, e.g., M.P.E.P. § 608.01(v) and the attached printouts from http://tess.uspto.gov/, notably the "PSOC" trademark registration information therein, and http://www.cypressmicro.com/corporate/CY_Announces_nov_13_2000.html). No new matter is introduced.

REMARKS

Claims 1-35 are presented for consideration in the present application, which is now believed to be in condition for examination. Early notice to that effect is earnestly solicited.

Respectfully submitted,

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Typed Drawing

Word Mark	**PSOC**
Goods and Services	IC 009. US 021 023 026 036 038. G & S: semiconductors devices; microprocessors; and integrated microelectronic devices in the nature of semiconductors devices
Mark Drawing Code	(1) TYPED DRAWING
Serial Number	75951037
Filing Date	March 3, 2000
Filed ITU	FILED AS ITU
Published for Opposition	November 12, 2002
Owner	(APPLICANT) Cypress MicroSystems, Inc. CORPORATION DELAWARE 12230 NE. Woodinville Drive Suite A Woodinville WASHINGTON 98072
Attorney of Record	John Weber
Type of Mark	TRADEMARK
Register	PRINCIPAL
Live/Dead Indicator	LIVE

CYPRESS MICROSYSTEMS UNVEILS PROGRAMMABLE SYSTEM-ON-A-CHIP FOR EMBEDDED INTERNET, COMMUNICATIONS AND CONSUMER SYSTEMS

PSoC™ Devices Integrate Programmable Analog and Digital Functions To Simplify Design Of Wireless, Handheld, Data Communications, and Industrial Systems

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WOODINVILLE, Wash., November 13, 2000 - Cypress MicroSystems, a subsidiary of Cypress Semiconductor, today introduced a family of programmable system-on-a-chip (PSoC™) devices, designed to implement a single, configurable device on MCU-based system boards. As general purpose solutions, PSoC devices are targeted for implementation in embedded applications, including audio, wireless, handheld, data communications, Internet control, industrial, and consumer systems.

PSoC devices integrate a fast microcontroller, SONOS™-based (Silicon Oxide Nitride Oxide Silicon) Flash memory and SRAM, and programmable arrays of analog and digital system functions - known as PSoC blocks - in low-cost, small-footprint packages. To save designers time, Cypress Microsystems also offers User Modules - pre-designed peripherals comprised of PSoC blocks. By selecting a PSoC with the needed resource combination of memory, PSoC blocks and pins, designers have a device that reduces costs by eliminating external chips and simplifying system design.

"Today there are thousands of different 8-bit microcontrollers on the market, and designers still have trouble finding one that is a perfect fit for their application. In addition, embedded applications require analog peripherals that usually call for additional external devices," said Mike Polen, Cypress MicroSystems's vice president of marketing. "Engineers know that the perfect solution is a custom-designed system-on-a-chip, but custom microcontrollers, ASICs and PLDs are expensive, require very large volumes or call for specialized design skills."

"In contrast, the Cypress Microsystems PSoC solution offers custom configurations, takes no time or special expertise to create, incurs no NRE, and integrates both analog and digital functions," continued Polen. "These factors make the cost of the PSoC solution competitive with standard microcontrollers."

SONOS - a proprietary Cypress process technology - is key to Cypress Microsystems's system-on-a-chip. SONOS is a cost-effective, electrically-erasable, programmable, non-volatile memory structure that speeds time-to-market at a cost that is comparable with commodity devices. SONOS is also being implemented in Cypress Semiconductor's frequency timing generators, USB controllers and intelligent control network devices.

About PSoC blocks and User Modules

After a review of the peripherals found in microcontrollers and the analog ICs used in typical designs, Cypress Microsystems engineers selected a variety of digital and analog peripherals, then created PSoC blocks, or system-on-a-chip blocks, and integrated them into each PSoC device. Users select the functions they need and configure the PSoC blocks on the PSoC device accordingly.

Digital PSoC blocks are 8-bit peripherals that can be programmed to perform a variety of functions by changing the contents of a few registers. They can be configured as timers, controllers, serial communications ports, CRC generators, or pseudo-random number generators. They can be connected in series to handle more complex functions - for example, a 24-bit timer is three connected 8-bit PSoC blocks acting as timers.

Analog PSoC blocks consist of programmable operational amplifier circuits that can be configured to perform a set of typical analog peripheral functions. Analog PSoC blocks can be programmed by setting a few registers to interconnect and trim the appropriate operational amplifier circuit to create the desired result. Among the typical peripherals that can be created are amplifiers, DACs, ADCs, analog drivers, and high-, low- and band-pass filters.

To eliminate the need for customers to understand PSoC blocks in-depth and further shorten development time, Cypress Microsystems developed User Modules, preconfigured peripherals created from PSoC blocks. User Modules allow customers to select the functions they need and automatically integrate the necessary PSoC

blocks into their PSoC device.

Software Support

Cypress Microsystems will offer PSoC Designer™, a complete development system to support the PSoC device. The system will include a C compiler and assembler, a linking and debugging tool, an in-circuit emulator, and the Device Editor™.

Designers can use the Device Editor and its graphical interface to configure a PSoC device by dragging the desired peripherals or functions - from a library of User Modules - into the part. The selected User Modules are then automatically mapped onto the available PSoC blocks.

On-chip Flash program memory stores each PSoC device's parameters, allowing the user to reprogram the device during production, during system test or in the field. PSoC devices may even be self-reprogrammed remotely.

"PSoC devices are like a screwdriver with replaceable bits," stated Nathan John, Cypress Microsystems's director of marketing. "They can be configured and reconfigured as the design progresses and functional requirements change. They provide a core set of analog and digital functions that eliminate the need for additional devices. And they can be programmed to custom-fit any application."

Availability and Pricing

Cypress Microsystems will initially offer the following PSoC devices:

Part Number	Max. Speed	Package	Samples	Production	Price (Q 1,000)
CY8C25122	24 MHz	8-pin DIP	Q1 2001	Q1 2001	$ 1.76
CY8C26233	24 MHz	20-pin DIP 20-pin SOIC 20-pin SSOP	Q1 2001	Q1 2001	$ 2.21
CY8C26443	24 MHz	28-pin DIP 28-pin SOIC 28-pin SSOP	Q4 2000	Q1 2001	$ 2.79
CY8C26643	24 MHz	48-pin DIP 48-pin SSOP 48-pin TQFP	Q1 2001	Q1 2001	$ 3.53

About Cypress Microsystems

Cypress Microsystems designs, develops, manufactures and markets high-performance, field programmable integrated micro-based solutions for high-volume embedded control functions in computer, communications, consumer and control applications. Established as a subsidiary of Cypress Semiconductor Corporation in the fourth quarter of 1999, Cypress Microsystems's stockholders are its employees and Cypress Semiconductor. The close association with Cypress Semiconductor allows access to their process and design technology, and field sales and applications forces. Cypress Microsystems is based near Seattle in Woodinville, Washington.

The Cypress Microsystems PsoC™ family of programmable system-on-a-chip devices will replace many MCU-based system boards with one single-chip, programmable PSoC. A single PSoC device provides a fast microcontroller, SONOS™ FLASH and SRAM memory, and configurable analog and digital peripheral blocks in a range of convenient pin outs and memory sizes. This new product family will bring the cost and time-to-market advantages of programmable technologies, such as CPLDs and FPGAs, to the emerging system-on-a-chip marketplace.

More information about Cypress Microsystems and its products can be accessed through its Web site at www.cypressmicro.com.

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Statements in this press release regarding Cypress Semiconductor's business that are not historical facts are "forward-looking statements" involving risks and uncertainties, including but not limited to: the effect of global economic conditions, shifts in supply and demand, market acceptance, the impact of competitive products and pricing, product development, commercialization and technological difficulties, and capacity and supply constraints. Please refer to Cypress Semiconductor's Securities and Exchange Commission filings for a discussion of such risks.